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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/914,474	08/29/2001	Akio Koyama	XA-9543	5348

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MILES & STOCKBRIDGE PC  
1751 PINNACLE DRIVE  
SUITE 500  
MCLEAN, VA 22102-3833

EXAMINER

ABRAHAM, FETSUM

ART UNIT PAPER NUMBER

2826

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicant(s)

09/914,474

Applicant(s)

KOYAMA, AKIO

Examiner

Fetsum Abraham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 October 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-46 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-46 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 122.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) Z.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

FETSUM ABRAHAM  
PRIMARY EXAMINER

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**Claims rejection**

The restriction requirement imposed on the application has now been lifted in response to applicant's communication in paper no 6.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims **22-26,34-37** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claim **22** recites the limitation "**the third wiring layer**" in claims 7-12. There is insufficient antecedent basis for this limitation in the claims.

Claim **23** recites the limitation "**the internal circuit region**" in claims 7-14. There is insufficient antecedent basis for this limitation in the claims.

Claims **34** recites the limitation "**in the field effect transistor not used**" in claim 34.. There is insufficient antecedent basis for this limitation in the claim.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims **1-21,27-33,38-46**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Akaogi et al (5,576,637).

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The patent discloses most aspect of the claimed invention in figures 36,37 a power terminal (250) for receiving power (V1) from external power supply is connected to a switch transistor inside an N-WELL whose result directly affects the NMOSFET in the P-WELL at its output (V2) level. The discussed structure of figure 37 is displayed in circuit configuration in figure (36) whose interdependent function in relation to the applied power supply is discussed in page 28, 15-25. In the structures, the line that connects node (250) with the active region of switch (248) is the power line analogous to the claimed power wiring.

As for claims 1,13,40,41 the switch and the transistor in the P-WELL are also separately formed in the same substrate. Although the structure presents a single circuit, it would have been obvious to one skilled in the art to duplicate the structure in multiplicity since integrated circuits are commonly formed on a single substrate as such to save material and reduce processing steps.

As for claims 2,4,7,8,11-15,17,45 the FET in the P-WELL is formed in a P-type semiconductor which is opposite to the N-WELL where the switch is discretely formed. Specifically as to the claims that indicate multiplicity of circuit elements, the issue here is the formation of the elements in multiplicity which is common in IC manufacturing for the reasons given above.

As for claims 3,5,9,10-12,16,46 the N and P regions of the FET and the switch that are not used in the power wiring connection are connected to each other at terminal (253).

As fore claim 6, the issue is substrate bias which can easily be wired to the power line depending on the polarity of power supplied. In the case of the patent, V1H and Vin are the

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substrate biases that could easily be connected to the power lines based on the polarity of the power signal in order to minimize circuit density.

As for claim 18, all cells or circuits in a given IC are not simultaneously used.

As for claim 19, MOSFETs are known elements used as clock circuits.

As for claim 20, the switch circuits are FETs.

As for claim 21, the transistors are N and P conductivity types.

As for claim 27, the claimed operation is normal to the prior art.

As for claims 28,29,43,44 any circuit in a given substrate can be duplicated. However, the duplication is not patentable since the patentable idea is already represented by the single circuit. In light of this observation, the claim language is a duplication of a single circuit. And that circuit is shown by the prior art. The difference here is that devices are organized according their conductivity types. However, it is common to form PMOSs on a different conductivity type substrates and NMOSs in the opposite.

As for claims 43,44 in specifics, there is always depletion capacitance formed between any PN layers at their junction.

As for claim 30, the multiple circuits in the claim and the connections claimed is shown by a single circuit configuration of the prior art.

As for claims 31,32, all the circuit configurations are already discussed by a single circuit configuration of the prior art. The only difference again is the multiplicity of the circuits.

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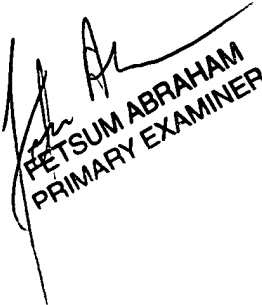
As for claims 33,34,38 the circuit configuration of the prior art has I/I terminals similar to all semiconductor devices.

Any inquiry concerning this communication should be directed to Fetsum Abraham at telephone number (703) 305,3793, or by E-mail at *fetsum.abraham@uspto.gov*.

Any inquiry of a general nature or relating to the status of this application should be directed to the *SPE of AU:2826* at (703)308-6601, or the *Group receptionist* at (703) 308-0956.

Fetsum Abraham

10/16/02

  
FETSUM ABRAHAM  
PRIMARY EXAMINER